

Appl. No. 10/716,309
Arndt. dated March 6, 2006
Reply to Office Action of September 6, 2005

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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

- 1 1. (Currently Amended) A method for placing circuit elements into logic
2 blocks, the method comprising:
 - 3 assigning each of the circuit elements to a separate abstract block, wherein the
4 circuit elements are part of a user design for a programmable integrated circuit and the abstract
5 block represents a functional attribute of its assigned circuit element;
 - 6 grouping each of the abstract blocks into a logic block based at least in part on a
7 correspondence between a functional attribute of the logic block and the functional attribute of
8 each abstract block;
 - 9 removing a first one of the abstract blocks from a the logic block in response to
10 placement information that indicates a design goal would be improved by rearranging at least a
11 portion of the user design; and
 - 12 placing the first abstract block into a different logic block on the programmable
13 integrated circuit, wherein the functional attribute of removed abstract block corresponds with a
14 functional attribute of the different logic block.
- 1 2. (Original) The method according to claim 1 wherein the design goal
2 includes routability and signal timing in the user design.
- 1 3. (Original) The method according to claim 1 wherein the circuit elements
2 include lookup tables and registers.
- 1 4. (Original) The method according to claim 1 wherein the circuit elements
2 include DSP blocks and RAM blocks.
- 1 5. (Original) The method according to claim 1 further comprising:

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2 determining whether placing each circuit element into the logic block violates any
3 of a set of design rules relating to the logic block, wherein the logic blocks are grouped into
4 clusters; and

5 determining whether placing each of the circuit elements into a cluster violates
6 any of a set of design rules relating to the cluster.

1 6. (Original) The method according to claim 5 wherein each of the abstract
2 blocks are grouped into a cluster based on an attraction of the abstract block to the cluster, and
3 the attraction measures a number of nets and connections of nets absorbed into the cluster if the
4 abstract block is placed inside the cluster.

1 7. (Original) The method according to claim 5 wherein each of the abstract
2 blocks are grouped into a cluster based on an attraction of the abstract block to the cluster, and
3 the attraction measures a number of timing critical connections absorbed into the cluster if the
4 abstract block is placed inside the cluster.

1 8. (Original) The method according to claim 5 further comprising:
2 placing one of the abstract blocks into another logic block within the cluster if
3 placing that abstract block into the logic block violates any of the design rules relating to the
4 logic block; and

5 placing one of the abstract blocks into another cluster if placing that abstract
6 block into the cluster violates any of the design rules relating to the cluster.

1 9. (Currently Amended) The method according to claim 1 wherein the logic
2 blocks implement functions performed by two lookup tables with less than an integer k unique
3 input variables; and the method further comprises:

4 determining whether grouping each of the abstract blocks into the logic block
5 placing each of the abstract blocks into the logic blocks causes any of the logic blocks to have
6 more than k unique input variables.

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1 10. (Original) The method according to claim 1 wherein the placement
2 information includes floorplanning information.

1 11. (Original) The method according to claim 1 wherein the placement
2 information includes partition information.

1 12. (Currently Amended) The method according to claim 1 wherein the
2 placement information includes data obtained by a previous placing placement of a portion of the
3 user design on the programmable integrated circuit.

1 13. (Original) The method according to claim 1 wherein:
2 grouping each of the abstract blocks into a logic block further comprises grouping
3 first and second abstract blocks into a first logic block;
4 removing the first one of the abstract blocks from the logic block further
5 comprises removing the first abstract block from the first logic block; and
6 placing the first abstract block into a different logic block further comprises
7 placing the first abstract block into a second logic block and placing the second abstract block
8 into the first logic block.

1 14. (Currently Amended) A computer program product stored on a computer
2 readable medium for placing circuit elements in a user design for a programmable integrated
3 circuit into logic blocks, the computer program product comprising:

4 computer program instructions for assigning each of the circuit elements to a
5 separate abstract block, wherein the abstract block represents a functional attribute of its assigned
6 circuit element;
7 computer program instructions for grouping each of the abstract blocks into
8 a logic block based at least in part on a correspondence between a functional attribute of the
9 logic block and the functional attribute of each abstract block;

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10 computer program instructions ~~code~~ for determining whether placement
11 information indicates that a design goal would be improved by moving at least one of the
12 abstract blocks into a different logic block; and
13 computer program instructions ~~code~~ for removing the at least one abstract block
14 from a first logic block and placing the at least one abstract block into a second logic block in
15 response to the determination based on the placement information, wherein the functional
16 attribute of the removed abstract block corresponds with a functional attribute of the different
17 logic block.

1 15. (Original) The computer program product as defined in claim 14 wherein
2 the design goal includes signal timing and routability in the user design.

1 16. (Currently Amended) The computer program product as defined in claim
2 14 wherein the logic blocks are grouped into clusters of logic blocks, and the computer program
3 instructions ~~code~~ for grouping each of the abstract blocks into a logic block further comprises
4 computer program instructions ~~code~~ for grouping each of the abstract blocks into a cluster of
5 logic blocks based on an attraction of the abstract block to the cluster.

1 17. (Currently Amended) The computer program product as defined in claim
2 16 further comprising:
3 computer program instructions ~~code~~ for determining whether grouping the
4 abstract blocks into the clusters violates any design rules of the clusters; and
5 computer program instructions ~~code~~ for determining whether grouping the
6 abstract blocks into the logic blocks violates any design rules of the logic blocks.

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1 18. (Original) The computer program product as defined in claim 14 wherein
2 some of the circuit elements are lookup tables, and some of the circuit elements are registers.

1 19. (Original) The computer program product as defined in claim 16 wherein
2 the attraction measures a number of nets and connections of nets absorbed into the cluster if the
3 abstract block is placed inside the cluster.

1 20. (Original) The computer program product as defined in claim 16 wherein
2 the attraction measures a number of timing critical connections absorbed into the cluster if the
3 abstract block is placed inside the cluster.

1 21. (Currently Amended) The computer program product as defined in claim
2 17 further comprising:

3 computer program instructions ~~code~~ for placing one of the abstract blocks into
4 another logic block if placing that abstract block to the logic block violates any of the design
5 rules relating to the logic block.

1 22. (Currently Amended) The computer program product as defined in claim
2 17 further comprising:

3 computer program instructions ~~code~~ for placing one of the abstract blocks to
4 another cluster if placing that abstract block to the first cluster violates any of the design rules
5 relating to the first cluster.

1 23. (Currently Amended) The computer program product as defined in claim
2 14 further comprising:

3 computer program instructions ~~code~~ for determining whether placing the abstract
4 blocks to the logic blocks causes any of the logic blocks have more than k unique input variables,
5 wherein the logic blocks are configurable to implement functions performed by
6 two lookup tables with less than k unique input variables.

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1 24. (Original) The computer program product as defined in claim 14 wherein
2 the placement information includes floorplanning information.

1 25. (Original) The computer program product as defined in claim 14 wherein
2 the placement information includes partition information.

1 26. (Original) The computer program product as defined in claim 14 wherein
2 the placement information includes data obtained by placing logic blocks that implement
3 portions of the user design on the programmable integrated circuit.

1 27. (New) The method of claim 1, wherein the logic block includes a first
2 functional attribute and a second functional attribute, and wherein grouping each of the abstract
3 blocks into a logic block further comprises:

4 assigning a first abstract block associated with a first circuit element to the first
5 functional attribute of the logic block; and

6 assigning a second abstract block associated with a second circuit element to the
7 second functional attribute of the logic block, such that the logic block is assigned the functional
8 attributes of the first and second circuit elements.

1 28. (New) The method of claim 27, wherein the first functional attribute of
2 the logic block includes a register and the functional attribute of the first circuit element includes
3 a register.

1 29. (New) The method of claim 27, wherein the second functional attribute of
2 the logic block includes a look-up table circuit adapted to implement a logic function and the
3 functional attribute of the first circuit element includes a logic function capable of being
4 implemented by the look-up table circuit.